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Claims

[c1] 1. A photolithography process of a thin film transistor (TFT) array substrate, comprising:
providing a mask, wherein the mask has a non-display element area and a display element area, wherein a plurality of stitching pixel patterns are disposed in a portion of the non-display element area adjacent to the display element area;
providing a substrate having a photoresist layer formed thereon;
setting the mask above a substrate;
blocking the display element area of the mask and performing an exposure process over the photoresist layer;
blocking the non-display element area of the mask and repeatedly performing exposure processes over the photoresist layer; and
performing a development process to pattern the photoresist layer, wherein a plurality of pixel patterns are formed in the photoresist layer corresponding to the display element area, a plurality of peripheral circuit patterns and a plurality of stitching pixel pattern are formed in the photoresist layer corresponding to the non-display element area, and wherein the stitching pixel

patterns and the pixel patterns are connected.

[c2] 2. The photolithography process of claim 1, further comprising a step of forming a plurality of driving element bonding patterns at an edge of the display element area of the mask.

[c3] 3. The photolithography process of claim 1, wherein the non-display element area of the mask is disposed at two edges of the display element area.

[c4] 4. A design of a mask for a thin film transistor (TFT) array substrate, wherein the mask has a display element area and a non-display element area, the mask comprising:
a plurality of pixel patterns disposed in a display element area;
a plurality of peripheral circuit patterns disposed in a non-display element area; and
a plurality of stitching pixel patterns disposed in a portion of the non-display element area adjacent to the display element area.

[c5] 5. The design of a mask of claim 4, further comprising a plurality of driving element bonding patterns disposed at an edge of the display element area.

[c6] 6. The design of a mask of claim 4, wherein the non-

display element area is disposed at two edges of the display element area.

[c7] 7. A thin film transistor (TFT) array substrate having a non-panel-display area and a panel-display area, comprising:
a plurality of pixel structures, disposed in a panel-display component;
a plurality of peripheral circuits, disposed in a non-panel-display area; and
a plurality of stitching pixel structures, disposed in the non-panel-display area, wherein the stitching pixel structures and the pixel structures are connected in the non-panel-display area.

[c8] 8. The thin film transistor (TFT) array substrate of claim 7, further comprising a plurality of driving element bonding areas disposed at an edge of the panel-display area.

[c9] 9. The thin film transistor (TFT) array substrate of claim 7, wherein the non-display element area is disposed at two edges of the display element area.

[c10] 10. A thin film transistor (TFT) array substrate having a non-panel-display area and a panel-display area, comprising:

a plurality of pixel structures, disposed in a panel-display component;

a plurity of first stitching pixel structures, disposed in the panel-display component, wherein the stitching pixel structures are adjacent to the pixel structures;

a plurality of peripheral circuits, disposed in a non-panel-display area; and

a plurality of second stitching pixel structures, disposed in the non-panel-display area, wherein the first stitching pixel structures of the panel-display component and the second stitching pixel structures of the non-panel-display area are connected in the non-panel-display area.